PAL timing (1)

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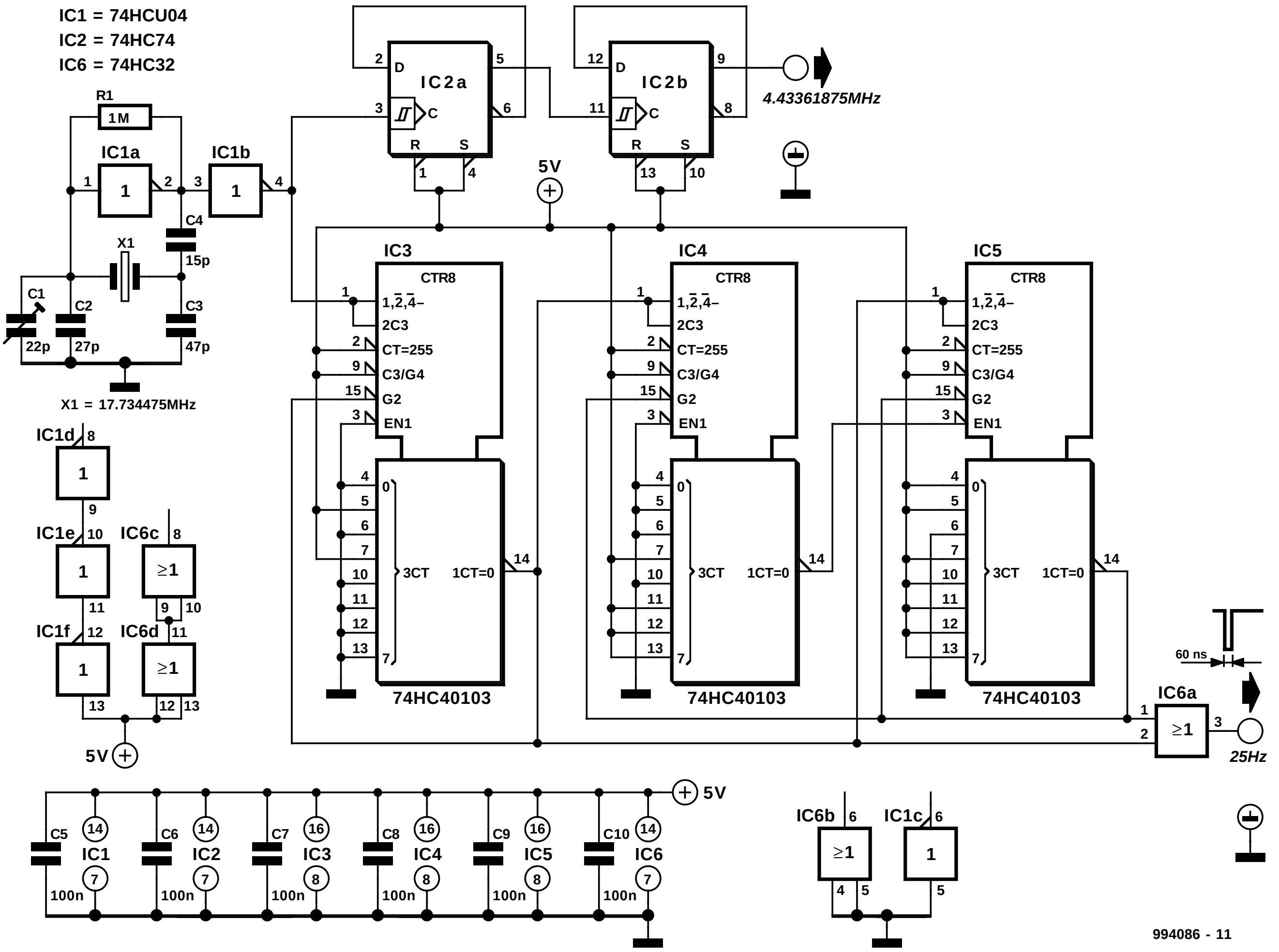

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This circuit is intended more as a design idea than as a finished project, in the light of the number of standard ICs that are employed.

In the PAL television system, the CCIR B and G standards specify that the colour carrier is directly coupled to the line rate, with a 25 Hz offset. The frequency ratio and offset are chosen to suppress interference patterns, according to the formula

$$f_{colour} = 283.75\ f_{line} + 25\ \text{Hz}$$

At a line rate of 15,625 Hz, this means that the PAL colour carrier frequency is 4.43361875 MHz. Single-sideband modulation is frequently used to obtain the correct relationship with the line rate. For example, the frequency of a crystal oscillator can be offset by 25 Hz, divided by 1135 and then multiplied by 8 to obtain twice the actual line rate. This is a rather complicated procedure, which we think could be made a lot simpler.

There is a fixed ratio between the 25 Hz frame rate and four times the colour carrier frequency. You can calculate this yourself —- four times the colour carrier frequency is exactly equal to 709,379 times the frame rate! An obvious approach is to use a crystal oscillator running at four times the colour carrier frequency and divide its output by 709,379 to obtain the frame rate. The line rate can then be derived from the frame rate with the help of a PLL circuit (see ‘PAL timing (2)’).

The crystal oscillator is a standard Pierce configuration with a trimmer capacitor, built around a 74HCU04 (IC1). The values of C2 and C3 must be properly chosen to obtain the specified load capacitance for the crystal. An incorrect value of C_{load} can make it impossible to adjust the oscillator to the exact frequency. Two D-type flip-flops wired as divide-by-two stages are used to obtain the colour carrier frequency.

Four ICs are used for the division needed to obtain the frame rate signal. IC3, IC4 and IC5 are presettable synchronous down-counters (type 74HC40103) that are very well suited for timing and frequency-division applications. The necessary division factor is split into two factors, namely 11 and 64,489. The 74HC40103 works as an (1 + N) divider, so value of 10 is applied to the preset inputs of IC3 for the first factor. The second factor is obtained by wiring IC4 and IC5 as a synchronous 16-bit divider, with the output of IC5 fed back to both synchronous preset inputs. The preset value is again 1 less than the division factor.

A disadvantage of the 74HC40103 is that glitches can occur, due to differences in internal delay times. These glitches are eliminated by clocking an OR gate (IC6a) at the divider output with the divider input signal. The 25 Hz output signal has an active low pulse approximately 60 ns long, which is essentially equal to one period of the crystal oscillator.

The current consumption of the circuit is a bit more than 12 mA, primarily due to IC1.

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